Amendments to the Claims

Claims 74-75 are cancelled, claims 1-34 were previously cancelled, and claims 35-73 were previously presented. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-34. (Cancelled)

35. (Previously presented) A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:

an input/output pad;

an output buffer adapted to receive output signals from the PLD, the output buffer modifying the output signals and being coupled to the input/output pad;

an input buffer adapted to receive a reference signal and input signals from the input/output pad and from the output buffer, the input buffer comparing the received input signals to the reference signal to produce a differential signal and coupling the differential signal to the PLD to provide the PLD with modified input signals; and

a plurality of programmable elements that select the standard with which the output buffer and the input buffer respectively modify the output and input signals.

36. (Previously presented) The programmable input/output device of claim 35, wherein the plurality of programmable elements further comprise:

a first programmable element coupled to the output buffer and the input buffer; and

a second programmable element coupled to the output buffer.

37. (Previously presented) The programmable input/output device of claim 36, wherein the plurality of programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, fuse and antifuse elements.

38. (Previously presented) The programmable input/output device of claim 35, wherein the input/output device provides signal modification in accordance with logic standards selected from the group consisting of TTL, CMOS, GTL, and HSTL.

39. (Previously presented) The programmable input/output device of claim 35, wherein the input buffer comprises:

a differential amplifier circuit being adapted to receive the input signals;

control circuitry that controls the modification of the input signals in accordance with the standard selected by the plurality of programmable elements; and

inversion circuitry that provides the modified input signals to the PLD.

40. (Previously presented) The programmable input/output device of claim 39, wherein the differential amplifier circuit and the control circuit operate in conjunction with each other to provide the modifications of the input signals in accordance with a plurality of logic standards.

41. (Previously presented) The programmable input/output device of claim 39, wherein the differential amplifier circuit and the input buffer operate independent of each other such that the modifications of the input signals are performed by the input buffer in accordance with a first logic standard and by the differential amplifier circuit in accordance with a second logic standard, the first and second logic standards being selected by the plurality of programmable elements.

42. (Previously presented) The programmable input/output device of claim 41, wherein the input buffer is optimized for speed to provide modification in accordance with the first logic standard at increased speed.

43. (Previously presented) The programmable input/output device of claim 41, wherein the differential amplifier circuit is optimized for speed to provide modification in accordance with the second logic standard at increased speed.

44. (Previously presented) A programmable input/output device for coupling a programmable logic device (PLD) to external circuitry, the input/output device comprising:

means for coupling the input/output device to the external circuitry;

means for receiving output signals from the PLD and for modifying the output signals in accordance with a selected logic standard, the means for receiving providing the modified output signals to the means for coupling;

means for modifying input signals received from the means for receiving and the means for coupling in accordance with the selected logic standard, the means for modifying including a means for comparing the received input signals to a reference signal to produce a differential signal and for providing the modified input signals to the PLD; and

means for selecting the selected logic standard from a plurality of logic standards.

45. (Previously presented) The programmable input/output device of claim 44, wherein the means for receiving comprises:

circuitry for modifying the output signals to an appropriate high voltage level in accordance with the selected logic standard if the output signals are logic high signals; and

circuitry for modifying the output signals to an appropriate low voltage level in accordance with the selected logic standard if the output signals are logic low signals.

46. (Previously presented) The programmable input/output device of claim 44, wherein the means for modifying comprises:

a first conversion circuit for converting the input signals in accordance with a first logic standard; and

a second conversion circuit for converting the input signals in accordance with a second logic standard.

47. (Previously presented) The programmable input/output device of claim 46, wherein the first and second conversion circuits are merged into a single conversion circuit.

48. (Previously presented) The programmable input/output device of claim 46, wherein the first and second conversion circuits are substantially independent of each other such that they may be independently optimized for operational speed improvements.

49. (Previously presented) A method for providing a programmable logic device (PLD) with the capability of being selectively coupled to external circuitry that operates in accordance with a selected one of a plurality of logic standards, the method comprising:

programmably selecting the selected one of a plurality of logic standards;

modifying output signals from the PLD in accordance with the selected logic standard such that high PLD signals correspond to high signals of the selected standard and low PLD signals correspond to low signal of the selected standard;

receiving input signals from an external interface;

comparing the received input signals to a reference signal to produce a differential signal in accordance with the selected logic standard such that high input signals are converted to high PLD signals and low input signals are converted to low PLD signals.

50. (Previously presented) The method of claim 49, wherein the programmably selecting further comprises selecting a logic standard selected from the group consisting of TTL, CMOS, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.

51. (Previously presented) The method of claim 49, wherein the programmably selecting further comprises applying a plurality of Select Bits to a plurality of programmable elements.

52. (Previously presented) A programmable input/output device capable of operating at multiple logic standards comprising:

an input/output terminal;

a plurality of programmable elements; and

an input buffer having circuitry controlled by at least one of the plurality of programmable elements to select between a first logic standard and a second logic standard wherein the second logic standard is a differential logic standard.

53. (Previously presented) The programmable input/output device of claim 52 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.

54. (Previously presented) The programmable input/output device of claim 52 wherein the first logic standard is a standard selected from the group consisting of TTL or CMOS.

55. (Previously presented) The programmable input/output device of claim 52 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.

56. (Previously presented) The programmable input/output device of claim 52 wherein the input buffer further comprises a differential amplifier circuit that is used for generating the differential logic standard.

57. (Previously presented) The programmable input/output device of claim 52 wherein at least one programmable element is coupled to the input buffer.

58. (Previously presented) The programmable input/output device of claim 52 further comprising an output buffer having circuitry controlled by at least one of the plurality of programmable elements to select between the first logic standard and the second logic standard.

59. (Previously presented) The programmable input/output device of claim 58 wherein the second logic standard is a differential logic standard.

60. (Previously presented) The programmable input/output device of claim 58 wherein at least one programmable element is coupled to the input buffer.

61. (Previously presented) The programmable input/output device of claim 60 wherein the input buffer and the output buffer are controlled by the same programmable element.

62. (Previously presented) A programmable input/output buffer capable of operating at multiple logic standards comprising:

an input/output terminal;

a plurality of programmable elements; and

an output buffer having circuitry controlled by at least one of the plurality of programmable elements to select between one logic standard and a differential logic standard.

63. (Previously presented) The programmable input/output device of claim 62 wherein the differential logic standard is a standard selected from the group consisting of HSTL and GTL.

64. (Previously presented) The programmable input/output device of claim 62 wherein the first logic standard is a standard selected from the group consisting of TTL and CMOS.

65. (Previously presented) The programmable input/output device of claim 62 wherein the programmable elements are elements selected from the group consisting of SRAM, EPROM, EEPROM, and antifuse elements.

66. (Previously presented) The programmable input/output device of claim 62 wherein at least one programmable element is coupled to the output buffer.

67. (Previously presented) The programmable input/output device of claim 62 further comprising an input buffer having circuitry controlled by at least one of the plurality of programmable elements to select between the first logic standard and the second logic standard.

68. (Previously presented) The programmable input/output device of claim 67 wherein the second logic standard is a differential logic standard.

69. (Previously presented) The programmable input/output device of claim 67 wherein at least one programmable element is coupled to the output buffer.

70. (Previously presented) The programmable input/output device of claim 69 wherein the input buffer and the output buffer are controlled by the same programmable element.

71. (Previously presented) A programmable input/output device comprising:

an input/output terminal;

an input buffer and an output buffer coupled to the input/output terminal, each of which includes means for modifying signals applied to the input/output terminal to a selected one of multiple logic standards wherein at least one of the multiple logic standards is a differential logic standard; and

a plurality of programmable elements for selecting the logic standard at which the input and output buffers operate.

72. (Previously presented) The programmable input/output device of claim 71 wherein the input buffer and the output buffer further comprise means for modifying signals applied to the input/output terminal to a logic standard selected from the group consisting of TTL, CMOS, GTL and HSTL.

73. (Previously presented) The input/output device of claim 71, wherein the input buffer and the output buffer share at least one programmable element.

74-75. (Cancelled)